**BUFFER ISSUE RESOLUTION DOCUMENT (BIRD)**

**BIRD NUMBER:** (for administrative use)

**ISSUE TITLE:** [Pin Reference]

**REQUESTOR:**  Walter Katz, Signal Integrity Software, Inc.

**DATE SUBMITTED:** (Draft 4/25/16)

**DATE REVISED:** (for administrative use)

**DATE ACCEPTED:** (for administrative use)

**DEFINITION OF THE ISSUE:**

All measurements or simulation results (“IBIS Data”) that are used to generate IBIS IV, VT, ISSO, and Thresholds are relative to a test fixture reference node or a simulator reference node (usually 0.0V or Node 0). During a simulation that uses IBIS Models, the IBIS specification is not clear what node should be used as the reference node. This is not an issue when the simulator supplies rail voltages (“\*\*\*\_ref”) to a model relative to the simulator reference node that are same as the reference voltages (“[\*\*\* Reference]”) supplied to the buffer when generating the IBIS Data. Some simulators use the terminal of the IBIS model that has a [\*\*\* Reference]=0.0V. This BIRD proposes a new [Component] section called [Pin Reference]. Each record after the keyword [Pin Reference] and until the end of the [Pin Reference] section shall contain two columns of data. The first column shall be a pin\_name, and the second column shall be a signal\_name. The signal\_name shall be the reference for the pin\_name, and the signal\_names that are are connected to the rail terminals of the model associated with the pin\_name.

**SOLUTION REQUIREMENTS:**

The IBIS specification must meet these requirements:

Table 1: Solution Requirements

|  |  |
| --- | --- |
| Requirement | Notes |
| 1. Allow an EDA tool to use IBIS model threshold in simulations where the voltages applied to a model rail terminals are not the same as the voltages applied to the rail terminals of the model when the “IBIS Data” is generated.
 |  |
|  |  |

(Enumerate each requirement in the table above, adding rows as needed.)

**SUMMARY OF PROPOSED CHANGES:**

For review purposes, the proposed changes are summarized as follows:

Table 2: IBIS Keywords, Subparameters, AMI Reserved\_Parameters, and AMI functions Affected

|  |  |  |
| --- | --- | --- |
| Specification Item | New/Modified/Other | Notes |
| New [Component] section [Pin Reference] | New | It is recommended, but not required, that there is a [Pin Mapping] section in the [Component]  |

**PROPOSED CHANGES:**

Add a new [Component] section called [Pin Reference]. Each record after the keyword [Pin Reference] and until the end of the [Pin Reference] section shall contain two columns of data. The first column shall be a pin\_name, and the second column shall be a signal\_name. The signal\_name shall be the reference for the pin\_name, and the signal\_names that are are connected to the rail terminals of the model associated with the pin\_name. The pin\_name must exist in the [Component] [Pin] section. The signal\_name must exist on at least one [Pin] in the [Component] [Pin] section, and the pin must have a Model\_name POWER or GND.

**BACKGROUND INFORMATION/HISTORY:**

IBIS is mostly a definition of the derivation of “IBIS Data” consisting of IV, VT, ISSO and voltage thresholds. For this, IBIS clearly defines the reference node used for thes voltages. IBIS contemplates the use of these models that where generated with the buffer supplied by specific rail voltages defined by the [Voltage Range], [Pullup Reference], [Pulldown Reference], [POWER Clamp Reference], [GND Clamp Reference], [Pullup Reference], and [External Reference] (“[\*\*\* Reference]”) keyword. These voltages are defined relative to the test fixture reference. When the model is simulated with voltages (relative to a simulator reference node) that do not have these same values applied to the models rail terminals, it is not defined in the specification how to compare the voltages at the buffer I/O (pin) terminal with the thresholds generated relative to test fixture reference. This BIRD address this confusion by specifying the signal name of a supply pin that the EDA tool can use to adjust the voltage measurement at the model I/O terminal that can be compared with the model thresholds.

**Appendix A – Template IBIS Specification Material**

*Keyword:* **[Pin Reference]**

*Required:* No

*Description:* The data after this keyword defines the signal\_name that an EDA tool shall use as the reference node for voltages at the pin.

*Sub-Params:* pin\_name, signal\_name

*Usage Rules:* The simulation node at the signal\_name shall be used as the reference node of measuremins at the pin\_name node when comparing simulation results with model thresholds.

[Pin Reference] It is recommended, but not requires that the [Component] has a [Pin Mapping] section.

Pin\_name must exist in the [Component] [Pin] section.

Signal\_name must exist in the [Component] [Pin] section on at least one pin\_name that has a model\_name POWER or GND.

*Other Notes:* If there is no [Pin Reference] section, or if a pin\_name in the component section does not have an entry in the [Pin Reference] section, and there is a model\_name on that pin that is not NC, POWER or GND, then the EDA tool must choose a reference node for simulation results at the pin\_name and rail terminals of the model. Some EDA tools use the simulater Node 0 as this reference. Other EDA tools use the rail terminal that has its Reference voltage [\*\*\* Reference] ([Pullup Reference], [Pulldown Reference], [POWER Clamp Reference], [GND Clamp Reference], [Pullup Reference], and [External Reference]) defined as 0.0V in the model.

When analyzing the waveforms at the buffer to compare them to such things as Vinl, Vinh, Vmeas and Receiver Thresholds, the voltage at the I/O Pin relative to the simulator reference node, must be adjusted by the difference of the voltage at the [Pin Reference] terminal relative to the simulator reference node and the value of the [\*\*\* Reference] at the [Pin Reference] terminal. Note that the “Reference\_supply” in the [Receiver Thresholds] section may not be the same rail signal\_name as the signal\_name in the [Pin Reference] for that buffer. The equation for the adjusted Vth must also supply this correction to the voltage at the Reference\_supply terminal relative to the simulator reference node.

*Example:*

[Component] SAME\_RAILS

 [Pin] signal\_name model\_name R\_pin L\_pin C\_pin

1 IO\_1 ECL\_0V

2 IO\_2 PECL\_5V

3 VCC POWER | 5V

4 VEE GND | 0V

5 VSS POWER | -5.0V

[Pin Mapping] pulldown\_ref pullup\_ref gnd\_clamp\_ref power\_clamp\_ref

1 VEE VEE VSS VEE | ECL\_0V

2 VCC VCC VEE VCC | PECL\_5V

3 NC VCC

4 VEE NC

5 NC VSS

[Pin Reference]

1 VEE

2 VEE

3 VEE

5 VEE

[Model] ECL\_0V

Model\_type I/O\_ECL

Vinh = -1.13V | 3.87V

Vinl = -1.48V | 3.52V

Vmeas = -1.29 | 3.71

Rref = 50.0

Cref = 0.0

Vref = -2.0 | 3.0

 [Voltage Range] 0.0V 0.0V 0.0V

| [Pullup Reference] 0.0V 0.0V 0.0V

| [Pulldown Reference] 0.0V 0.0V 0.0V

| [POWER Clamp Reference] 0.0V 0.0V 0.0V

| [GND Clamp Reference] 0.0V 0.0V 0.0V

[GND Clamp Reference] -5.0V -5.0V -5.0V

|

[Model] PECL\_5V

Model\_type I/O\_ECL

Vinh = 3.87V

Vinl = 3.52V

Vmeas = 3.71

Rref = 50.0

Cref = 0.0

Vref = 3.0

 [Voltage Range] 5.0V 4.5V 5.5V

[Pullup Reference] 5.0V 4.5V 5.5V

[Pulldown Reference] 5.0V 4.5V 5.5V

[POWER Clamp Reference] 5.0V 4.5V 5.5V

| [GND Clamp Reference] 5.0V 4.5V 5.5V